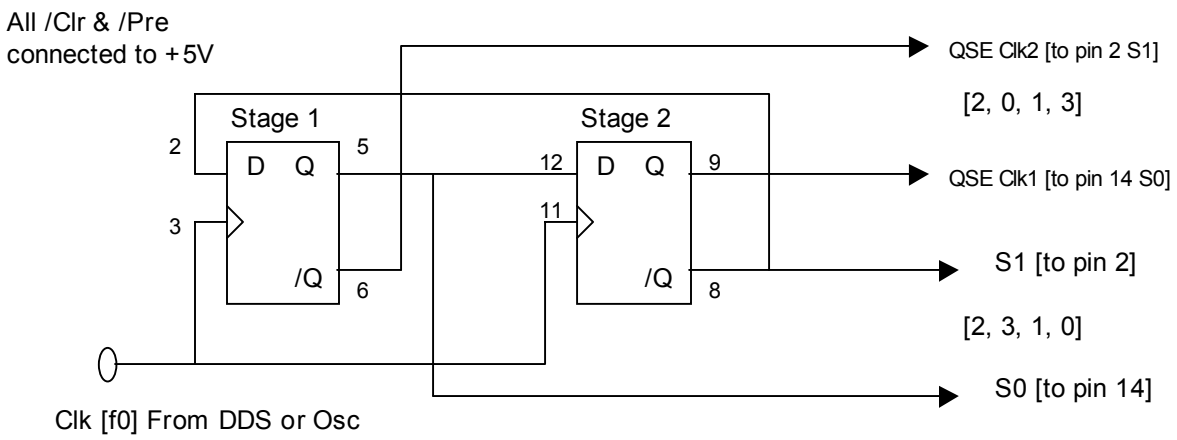
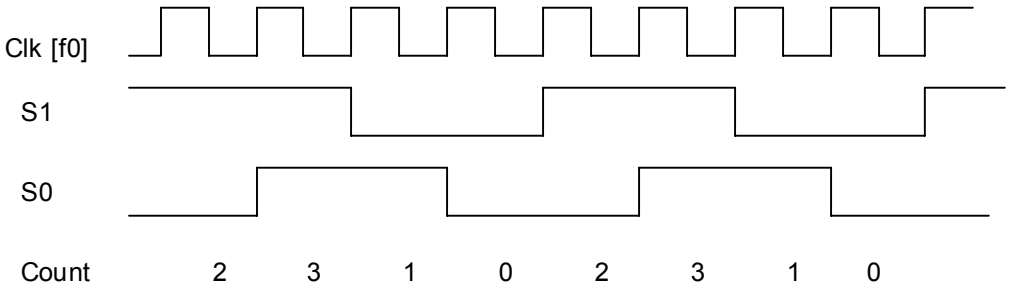
Softrock Synchronous Clock Generators from $4xF_0$ Clocks

Two Stage [typ] 74xxx74 Synchronous Clock
To drive [typ] FST3253



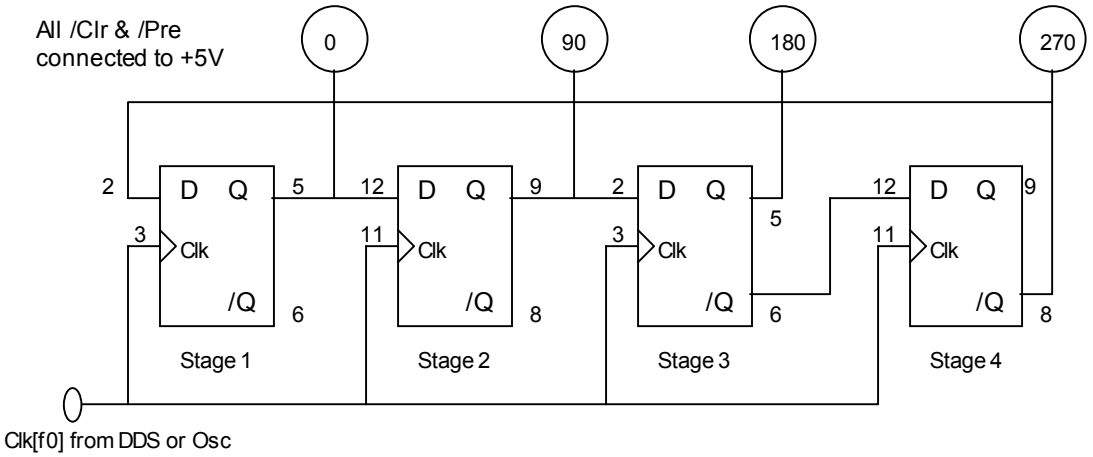


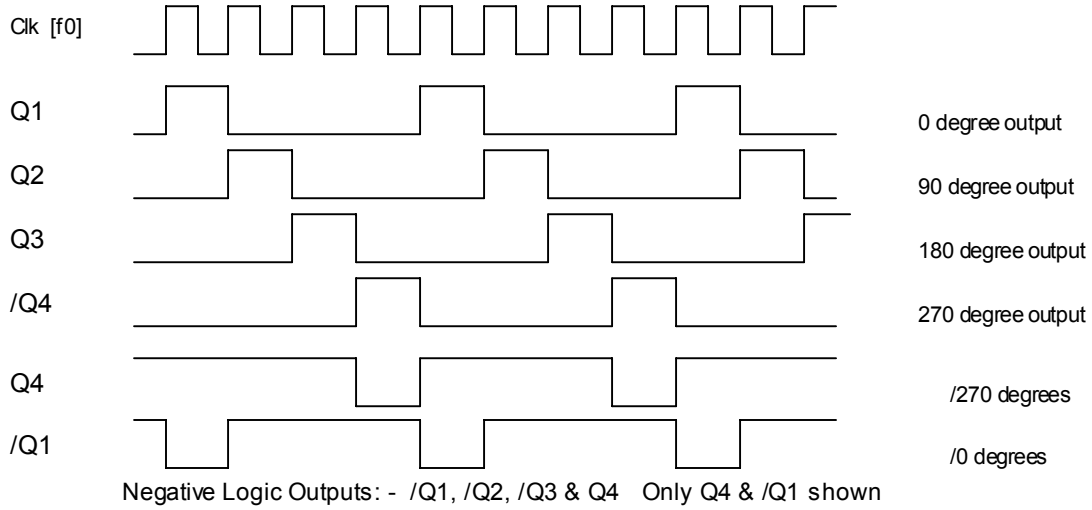
Two Stage State Diagram

[from]	[f_0]	[/Q_2]			[Q_1]		
State	Clk	D_1	Q_1	/Q_1	D_2	Q_2	/Q_2
Pwr Up	x	1	0	1	0	0	1
nt_0^-	x	↘			↘		
1st clk	↑	1	1	0	1	0	1
2nd	↑	0	1	0	1	1	0
3rd	↑	0	0	1	0	1	0
4th	↑	1	0	1	0	0	1
5th	↑	1	1	0	1	0	1
6th	↑	0	1	0	1	1	0
7th	↑	0	0	1	0	1	0
8th	↑	1	0	1	0	0	1
Pin #			**5**	**6**		**9**	**8**
Outputs			**[S_0]**	**[Clk_2]**		**[Clk_1]**	**[S_1]**

Softrock Synchronous Clock Generators from $4xF_0$ Clocks

Four Stage [typ] 74xxx74 Synchronous Clock
To drive [typ] FST3125





Negative Logic Outputs: - /Q1, /Q2, /Q3 & Q4 Only Q4 & /Q1 shown

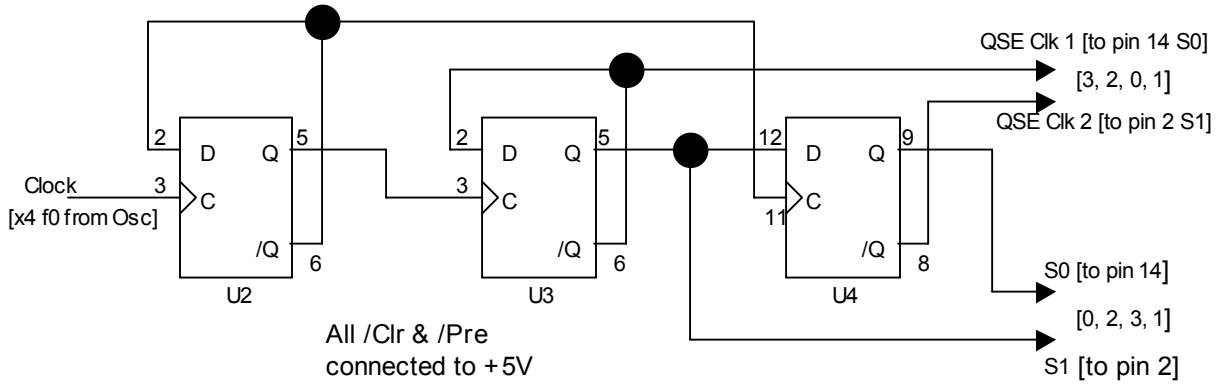
4 Stage State Diagram

[from]	[f_0]	[$/Q_4$]			[Q_1]			[Q_2]			[$/Q_3$]		
State	Clk	D_1	Q_1	$/Q_1$	D_2	Q_2	$/Q_2$	D_3	Q_3	$/Q_3$	D_4	Q_4	$/Q_4$
Pwr Up	x	1	0	1	0	0	1	0	0	1	1	0	1
nt_0^-	x	↘			↘			↘			↘		
1st clk	↑	0	1	0	1	0	1	0	0	1	1	1	0
2nd	↑	0	0	1	0	1	0	1	0	1	1	1	0
3rd	↑	0	0	1	0	0	1	0	1	0	0	1	0
4th	↑	1	0	1	0	0	1	0	0	1	1	0	1
5th	↑	0	1	0	1	0	1	0	0	1	1	1	0
6th	↑	0	0	1	0	1	0	1	0	1	1	1	0
7th	↑	0	0	1	0	0	1	0	1	0	0	1	0
8th	↑	1	0	1	0	0	1	0	0	1	1	0	1
9th	↑	0	1	0	1	0	1	0	0	1	1	1	0
10th	↑	0	0	1	0	1	0	1	0	1	1	1	0
11th	↑	0	0	1	0	0	1	0	1	0	0	1	0
Outputs			0°			90°			180°				270°

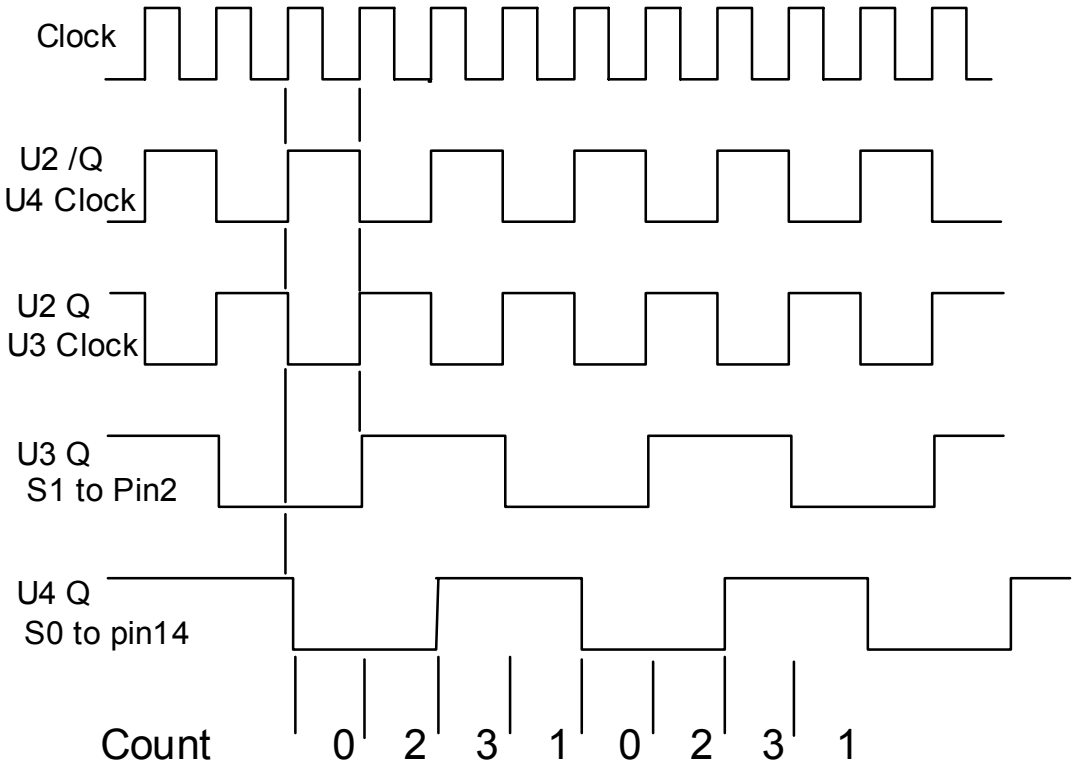
Softrock Synchronous Clock Generators from $4xF_0$ Clocks

Reference 74HC74 Design

Softrock asynchronous clock generator v6.2 Lite & RXTX



Asynchronous clocking for receiver [transmitter is similar but 3, 2, 0, 1]



Note: Clock edges do not match up on S_0 and S_1 – that is why it is asynchronous